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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,959	06/20/2001	Hidemasa Zama	210067US-2	2668

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EXAMINER
TAN, VIBOL

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/883,959	ZAMA ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-7,11-13,15 and 17* is/are allowed.

6)☒ Claim(s) *1,3,4,8-10,14 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *20* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1, 3, and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwaki et al. (U.S. PAT. 6,208,170).

In claim 1, Iwaki et al. teaches all claimed features in Fig. 3, a semiconductor integrated circuit comprising: a plurality of gate circuits (101, 103, 102); and a control circuit (clock generator not shown) configured to control the operation of some gate circuits (101, 102) among said plurality of gate circuits (101, 103, 102), each of said some gate circuits among said plurality of gate circuits including: a logic circuit constituted by a plurality of first transistors (inherent NMOS transistors located inside 101 and 102); and a switch circuit which includes second (104) and third (105)

transistors controlled to turn on/off by said control circuit, each having a threshold voltage higher (col. 4; lines 28, 39) than that of each of said first transistors and conductive types different from each other, said switch circuit being capable of cut off said logic circuit from a power supply line (VCC) by simultaneously turning off said second and third transistors (when SLP is at logic 1 SLPB is at logic 0, 104 and 105 are both cut OFF), wherein said some gate circuits are provided on a critical path (101 is on the critical path).

Iwaki et al. teaches all claimed features of claims 3 and 4 in Figs. 3 and 4, a logic operation circuit comprising: a gate circuit (102) which is connected between a virtual voltage line (QVCC) and a first reference voltage line (VSS) and constituted by a plurality of first transistors (LOW Vth LOGIC CIRCUIT); and a second transistor (104) which is connected between a second reference voltage line (VCC) and said virtual voltage line and constituted by a transistor having a threshold voltage higher (col. 4, line 28) than that of each of said first transistors, a source/drain terminal of each of said first transistors in said gate circuit being connected to either a source/drain terminal of another first transistor in said gate circuit (the same manner to the connections inside 301 in Fig. 4) or an output terminal (output from 102) of said gate circuit, wherein said logic operation circuit defined in claim 3 is provided on a critical path.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by JP-6-29834.

In claims 8-10, JP-6-29834 teaches all claimed features in Fig. 1, a logic operation circuit comprising: a gate circuit (20) which is constituted by a plurality of first transistors (T21, T22) and connected to first and second virtual voltage lines (CSB, CS); a second transistor (TS1) which is connected between a first reference voltage line (VDD) and said first virtual voltage line and has a threshold voltage higher than said first transistors; a third transistor (TS2) which is connected between a second reference voltage line and said second virtual voltage line and has a threshold voltage higher than that of each of said first transistors; and a storage circuit (30) capable of holding output logic of said gate circuit, said storage circuit being composed of transistors having threshold voltages higher than that of each of said first transistors, said second and third transistors being controlled to be OFF when said storage circuit holds said output logic of said gate circuit, and said second and third transistors being controlled to be ON when said storage circuit does not hold said output logic of said gate circuit, wherein a source/drain terminal of said first transistor in said gate circuit is connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal of said gate circuit, wherein said logic operation circuit is provided on a critical path.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwaki et al. in view of JP-6-29834.

In claim 14, Iwaki et al. teaches in Figs. 1 and 2, a Flip flop comprising: a first conduction interception circuit (301, 304, 305) capable of switching conduction or shutoff between an input terminal (→) and an output terminal (→); a first storage (303) circuit capable of holding output logic of said first conduction interception circuit; a second conduction interception circuit (302, 304, 305) which is capable of switching conduction or shutoff between an input terminal and an output terminal, and has said input terminal being connected to an output terminal of said first storage circuit; and a second storage circuit (shown by dashed lines, would be another storage circuit after 302) capable of holding output logic of said second conduction interception circuit, said first and second conduction interception circuits includes: a gate circuit (301 or 302) which is connected between a virtual voltage line (QVCC) and a first reference voltage line (VCC) and constituted by a plurality of first transistors (LOW Vth LOGIC CIRCUIT); and a second transistor (305) which is connected between a second reference voltage line (VSS) and said virtual voltage line (QVSS) and constituted by a transistor having a threshold voltage higher than that of each of said first transistors, a source/drain terminal of each of said first transistors in said gate circuit being connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal of said gate circuit; with the exception of teaching said first and second storage circuits being constituted by transistors having a threshold voltage higher than those of said

gate circuits in said first and second conduction interception circuits. However, JP-6-29834 teaches in Fig.1, storage circuit 30 being constructed by transistors having threshold voltage higher than those in the gate circuits.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to modify the device of Iwaki et al. by replacing the storage circuits with all transistors having high threshold voltages, as taught in JP-6-29834, in order to prove a semiconductor integrated circuit capable of reducing the chip size while assuring a low power dissipation.

In claim 16, Iwaki et al. teaches in Figs. 1 and 2, a Flip flop comprising: a first conduction interception circuit (301, 304, 305) capable of switching conduction or shutoff between an input terminal (→) and an output terminal (→); a first storage (303) circuit capable of holding output logic of said first conduction interception circuit; a second conduction interception circuit (302, 304, 305) which is capable of switching conduction or shutoff between an input terminal and an output terminal, and has said input terminal being connected to an output terminal of said first storage circuit; and a second storage circuit (shown by dashed lines, would be another storage circuit after 302) capable of holding output logic of said second conduction interception circuit. JP-6-29834 teaches in Fig. 1 the first and second conduction interception circuits includes: a gate circuit (20) which is constituted by a plurality of first transistors (T21, T22) and connected to first and second virtual voltage lines (CSB, CS); a second transistor (TS1) which is connected between a first reference voltage line (VDD) and said first virtual voltage line and has a threshold voltage higher than said first transistors; a third

transistor (TS2) which is connected between a second reference voltage line and said second virtual voltage line and has a threshold voltage higher than that of each of said first transistors; and a storage circuit (30) capable of holding output logic of said gate circuit, said storage circuit being composed of transistors having threshold voltages higher than that of each of said first transistors, said second and third transistors being controlled to be OFF when said storage circuit holds said output logic of said gate circuit, and said second and third transistors being controlled to be ON when said storage circuit does not hold said output logic of said gate circuit.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to modify the device of Iwaki et al. by replacing the storage circuits with all transistors having high threshold voltages, as taught in JP-6-29834, in order to prove a semiconductor integrated circuit capable of reducing the chip size while assuring a low power dissipation.

7. Claims 5-7, 11-13, 15, and 17 are allowed.

Response to Arguments

Applicant's arguments with respect to claim 1 been considered but is moot in view of the new ground(s) of rejection. The arguments with respect to claims 3 and 8 are not persuasive. Applicant have not responded to the Final Rejection for claims 14 and 16.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (703) 306-5948. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-6251 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0959.

Vibol Tan

Patent Examiner, AU 2819